A: A common way to make this kind of design more readable is to use proper design structuring. Here I have set up a block diagram that looks like this: The black boxes are the states of the registers, which are abstracted by the signals. If you put proper names on the signals, it should be easier to work with. This is a description of the circuit, using the same signals: Here is a state diagram of the circuit: In addition to these signals, I chose to add a clock signal and some time signals. This allows the simulation to show you what happens on each clock edge. You can see that on the output of the D flip flop, there is a signal. This signal is the sum of the two inputs, divided by two. You can also see that there is a second signal on the D flip flop, which is the carry signal. This is represented by \$Q\$ at the bottom of the diagram. You can also see that there is a D flip flop at the top left, where the inputs are shifted in, and another D flip flop where the carry in is added. If you add these together, you get the result. \$C\$ is the carry out from the adder. If you look carefully at this diagram, you can see that there are two paths between the top left and the bottom right, and the paths for both carry and non-carry are shown. Because the outputs of the D flip flops are the inputs of the next D flip flop, the paths are the same, and only the order is different. The main difference is that in the non-carry path, the carry input is shifted into the D flip flop on the left (the top left in the image), and then added to the result of the D flip flop on the right. Because the carry signal is a signal that is always high, it is represented in the state diagram by \$\overline{Q}\$ in the image, which is another way to say that \$Q\$ is always \$1\$ or \$0\$. You can see that the non-carry signal \$\overline{D_1}\$ is a \$1\$ for the carry in of the bottom right D flip flop, and \$\overline{D_2}\$ is a \$0\$ for the

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